

# Texas Instruments Power Management Reference Guide for Xilinx® FPGAs and CPLDs

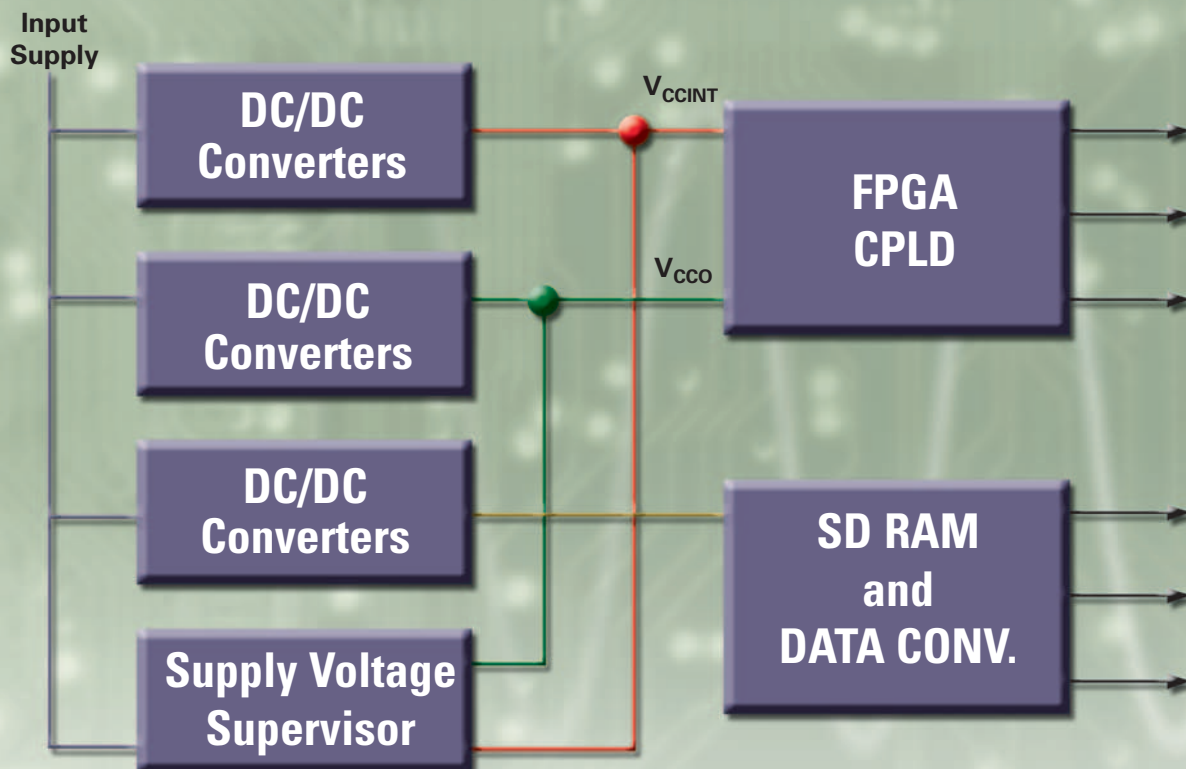
4Q 2005

## Includes:

- Power requirements of Xilinx FPGAs and CPLDs in typical applications
- Recommended Texas Instruments DC/DC converters for powering Xilinx FPGAs and CPLDs (Xilinx endorsed)
- DC/DC converters selection considerations
- Texas Instruments power management reference designs and design considerations
  - **Spartan™-3/3E/3L**
  - **Spartan™-IIE**
  - **Spartan™-II**
  - **Virtex™-II**
  - **Virtex-II Pro™**
  - **Virtex™-4**
  - **CoolRunner™-II**
- Texas Instruments product selection guides

[power.ti.com/xilinfpga](http://power.ti.com/xilinfpga)

## Powering Your FPGAs and CPLDs With TI's Power Management Products



## Power Requirements of Xilinx Solutions in Typical Applications

This information is intended to provide the designer with a general understanding of the power steady state requirements of Xilinx FPGA and CPLD families in typical applications. Please refer to the Xilinx Power Estimators, available at [www.xilinx.com/power](http://www.xilinx.com/power), for closer approximations specific to individual FPGA and CPLD devices and applications.

Power Requirements of Xilinx FPGA and CPLDs Families							
	Spartan™-II	Spartan™-IIE	Spartan™-3/3E/3L*	Virtex™-II	Virtex-II Pro™	Virtex™-4	CoolRunner™-II
V <sub>CCINT</sub> (core)	2.5 V ±5% @ 200 mA to 2 A	1.8 V ±5% @ 200 mA to 2 A	1.2 V ±5% @ 200 mA to 5 A	1.5 V ±5% @ 300 mA to 10 A	1.5 V ±5% @ 300 mA to 10 A	1.2 V ±5% @ 200 mA to 5 A	1.8 V ±5% @ 15 mA to 150 mA
V <sub>CCO</sub> (I/O)	3.3 V, 2.5 V and/or 1.5 V ±5% @ 50 mA to 500 mA	3.3 V, 2.5 V, 1.8 V and/or 1.5 V ±5% @ 50 mA to 500 mA	3.3 V, 3.0 V, 2.5 V, 1.8 V, 1.5 V and/or 1.2 V ±5% @ 50 mA to 6 A	3.3 V, 2.5 V, 1.8 V and/or 1.5 V ±5% @ 50 mA to 3 A	3.3 V, 2.5 V, 1.8 V and/or 1.5 V ±5% @ 50 mA to 3 A	3.3 V, 3.0 V, 2.5 V, 1.8 V, 1.5 V and/or 1.2 V ±5% @ 50 mA to 1.5 A	3.3 V, 2.5 V, 1.8 V, and/or 1.5 V ±7% @ 65 mA to 550 mA
V <sub>CCAUX</sub>	—	—	2.5 V ±5% @ 600 mA (max)	3.3 V ±5% @ 300 mA (max)	2.5 V ±5% @ 300 mA (max)	2.5 V ±5% @ 300 mA (max)	—
Digital Voltages above. Analog voltages for RocketIO™ Multi-Gigabit Transceiver (MGT) below.							
AV <sub>CCAUTX</sub>	—	—	—	—	2.5 V ±5% @ 60 mA/MGT	1.2 V ±5% @ 113 mA	—
AV <sub>CCAUXRX</sub>	—	—	—	—	2.5 V ±5% @ 35 mA/MGT	1.2 V ±5% @ 160 mA	—
AV <sub>TTX</sub>	—	—	—	—	1.8 V to 2.625 V @ 15 mA/MGT	1.2 V to 1.575 V @ 50 mA	—
AV <sub>TRX</sub>	—	—	—	—	1.8 V to 2.625 V @ 30 mA/MGT	1.0 V to 2.625 V @ 12 mA	—

## TI's Power Reference Designs for Xilinx FPGAs and CPLDs

- Spartan-II/Spartan-IIE..... Pages 4 - 5
- Spartan-3/3E/3L ..... Pages 5 - 7
- Virtex-II/ Virtex-II Pro..... Pages 8 - 10
- Virtex-4..... Pages 11 - 12
- CoolRunner-II..... Pages 13 - 14

Complete schematics, bills of materials and additional designs available at:

[power.ti.com/xilinxfpga](http://power.ti.com/xilinxfpga)

Questions? [fpgasupport@list.ti.com](mailto:fpgasupport@list.ti.com)

### Important Design Considerations:

- The shown power solutions are for applications guidance. Please visit the TI website for the latest updated information.
- Startup currents for charging bulk and decoupling capacitors can be large. Each design includes two or more of the following good power supply design practices to prevent these currents from forcing the point-of-load converter into thermal shutdown and/or excessively loading the input supply, either of which could prevent the point-of-load converter from reaching regulation.
  - Integrated high threshold under-voltage lockout (UVLO) circuit or external SVS to prevent the converter from turning on until the input supply reaches regulation.
  - Soft-starting each power rail, especially for fast-starting linear regulations.
  - Sequencing of the power rails, even though not explicitly by the FPGA.
- V<sub>CCAUX</sub> powers time-critical resources in the FPGA, including the Digital Clock Managers (DCMs). Therefore, this supply voltage is especially susceptible to power supply noise. V<sub>CCAUX</sub> can share a power plane with V<sub>CCO</sub>, but only if V<sub>CCO</sub> does not have excessive noise. Changes in V<sub>CCAUX</sub> voltage beyond 200 mV peak-to-peak should take place at a rate no faster than 10 mV per milli-second.
- These designs meet Xilinx's V<sub>CCINT</sub> and V<sub>CCO</sub> startup profile requirements, where applicable, including monotonic voltage ramp, current and power voltage ramp time requirements.
- The designs show the most common V<sub>CCO</sub> voltages, 2.5 V or 3.3 V. Other voltages can be supported by interchanging the depicted DC/DC converter with devices from the same family, assuming that the linear regulator does not exceed its power dissipation rating. Refer to the selection guides on pages 16 - 17 for alternatives.
- Only the minimum input and output capacitors for each IC are given in the schematics. Larger bulk and/or bypass capacitors will be required between the input supply and DC/DC converters depending on the placement of the input supply relative to the converters. Each FPGA also requires a minimum amount of bypass capacitance on each power rail as specified by Xilinx.

## TI Recommended DC/DC Converters for Powering Xilinx FPGAs and CPLDs

	Digital Voltages				Analog Voltages
	Low Dropout (LDO) Linear Regulators to 3 A	Switching DC/DC Converters (Integrated FET) to 9 A	Switching DC/DC Controllers (External FET) to 20 A	Switching DC/DC Modules to 30 A	Low Dropout (LDO) Linear Regulators to 1.5 A
<b>Spartan™-II</b>	TPS75003 TPS79xxx TPS786xx TPS703xx UC382-x	TPS54xxx	TPS6420x TPS400xx	PTH Series	—
<b>Spartan™-IIE</b>	TPS75003 TPS79xxx TPS786xx TPS703xx UC382-x	TPS54xxx	TPS6420x TPS400xx	PTH Series	—
<b>Spartan™-3/3E/3L</b>	TPS75003 TPS79xxx TPS786xx TPS704xx UC382-x	TPS54xxx	TPS6420x TPS400xx	PTH Series	—
<b>Virtex™-II</b>	TPS75003 TPS79xxx TPS786xx	TPS54xxx	TPS51020 TPS6420x TPS400xx TPS75003	PTH Series	—
<b>Virtex-II Pro™</b>	TPS75003 TPS79xxx TPS786xx	TPS54xxx	TPS51020 TPS6420x TPS400xx TPS75003	PTH Series	UC3821 TPS79xxx TPS786xx
<b>Virtex™-4</b>	TPS79xxx TPS786xx TPS75003	TPS54xxx	TPS51020 TPS75003	PTH Series	UC3821 TPS79xxx TPS786xx
<b>CoolRunner™-II</b>	TPS799xx TPS736xx TPS712xx	TPS61020 TPS61130	—	—	—

TI Linear Regulators require additional circuitry in order to provide soft-start on power-up. These recommended DC/DC converter products have been tested and endorsed by Xilinx to power the listed FPGAs. Digital voltages may be powered by either linear or switching DC/DC regulators. Analog voltages require linear regulators for minimal noise. Please see the selection guides on pages 16 and 17 for electrical specifics of the recommended devices.

## DC/DC Converter Selection Considerations

### • Low Dropout (LDO) Linear Regulators

- Easiest, smallest, and most cost-effective type of DC/DC converter to implement.
- Typically just requires the addition of a small input capacitor and output capacitor for stability.
- Exhibit low noise and therefore are ideal for powering analog voltages.
- Recommended for low power applications only due to generally low efficiency ( $LDO\ Eff = V_{OUT}/V_{IN} \times 100\%$ ) and resulting heat. Ensure the application does not violate the regulator's maximum allowable power dissipation. Refer to [TI Application Note SLVA118 'Digital Designer's Guide to Linear Voltage Regulators and Thermal Management'](#) for guidance.
- Low dropout performance needed to support small  $V_{IN}$  to  $V_{OUT}$  voltage differential.

### • Switching DC/DC Converters

- Easiest, smallest, discrete IC, switching DC/DC solution to implement due to integration of the FETs.
- Require the addition of an inductor and capacitors for the output filter.
- Use fixed output voltage, internally compensated devices to minimize component count and simplify implementation.
- Using adjustable output voltage TPS54xxx devices instead of fixed output options allows for external

compensation, resulting in a smaller solution due to the ability to minimize the inductor and use ceramic capacitors.

- Exhibit switching noise.
- Up to 95% efficient, giving a much cooler solution than a linear regulator, but due to the power dissipation in the internal FETs, switching DC/DC converters support only up to about 9 A.

### • Switching DC/DC Controllers

- More cost-effective than DC/DC converters, but consume more board space and are more challenging to implement as they require the addition of external FETs.
- Can support high-current applications, limited only by the controller's drive and the external FET's power dissipation capabilities.

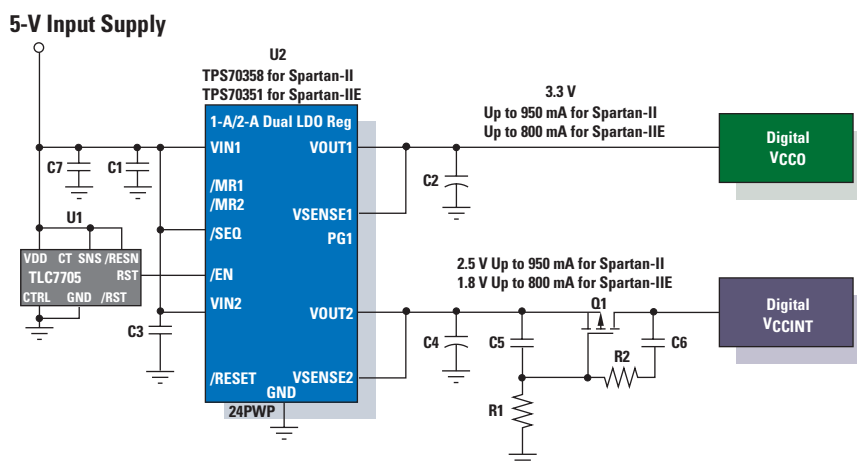
### • Modules

- Easiest switching DC/DC solution available. The module solution is complete, needing only the addition of an input and output capacitor for stability.
- Double-sided modules save board space.
- Full environmental qualification and EMI reports are available.

## Spartan™-II/ Spartan™-IIE Design 1

### Dual-Channel Low Dropout (LDO) Linear Regulator-Based, 800-mA $V_{CCINT}$ Solution for Spartan-IIE, 950-mA $V_{CCINT}$ Solution for Spartan-II

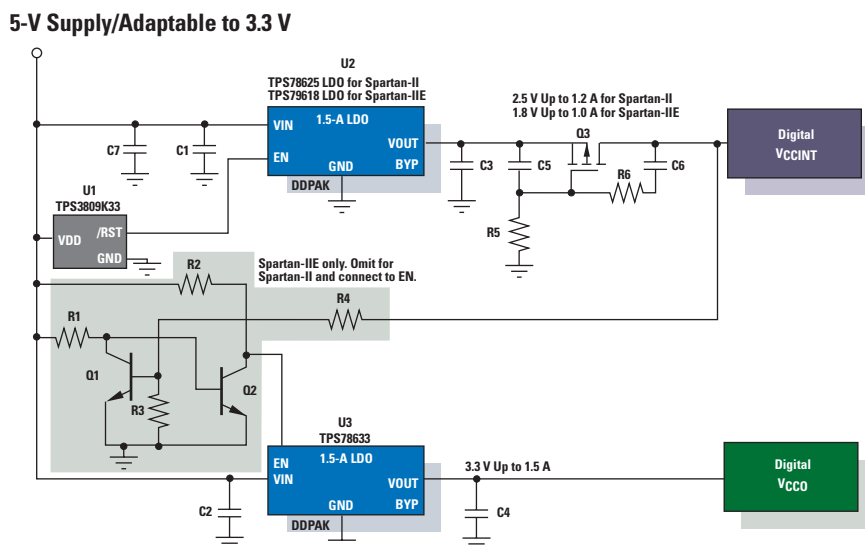
- Dual channel LDO in PowerPAD™ package saves cost and space.
- U1 monitors the input supply.
- Q1 is used to provide soft-start to  $V_{CCINT}$ .
- Sequencing  $V_{CCO}$ , then  $V_{CCINT}$ .
- U2 is limited to 2 W @  $T_A = 55^\circ\text{C}$  and no airflow due to power dissipation. Its maximum output current is split between the rails.



## Spartan™-II/ Spartan™-IIE Design 2

### Single-Channel LDO-Based, 1-A $V_{CCINT}$ Solution for Spartan-IIE, 1.2-A $V_{CCINT}$ Solution for Spartan-II

- Independent linear regulators allow higher power dissipation than an integrated dual-channel solution.
- Linear regulator solution saves cost and space over switching DC/DC solution.
- U1 monitors the input supply.
- Q3 is used to provide monotonic soft-start to  $V_{CCINT}$ .
- Sequence is  $V_{CCINT}$  then  $V_{CCO}$ .
- U2 is current limited @  $T_A = 55^\circ\text{C}$  and no airflow, due to power dissipation.
- Reduce cost by using lower current LDOs from U2, U3.
- Adapt to 3.3-V input:
  - Omit U3
  - Replace TPS3809K33 with TPS3809L30
  - With the lower  $V_{IN}$  to U2, the LDO can now support higher currents.

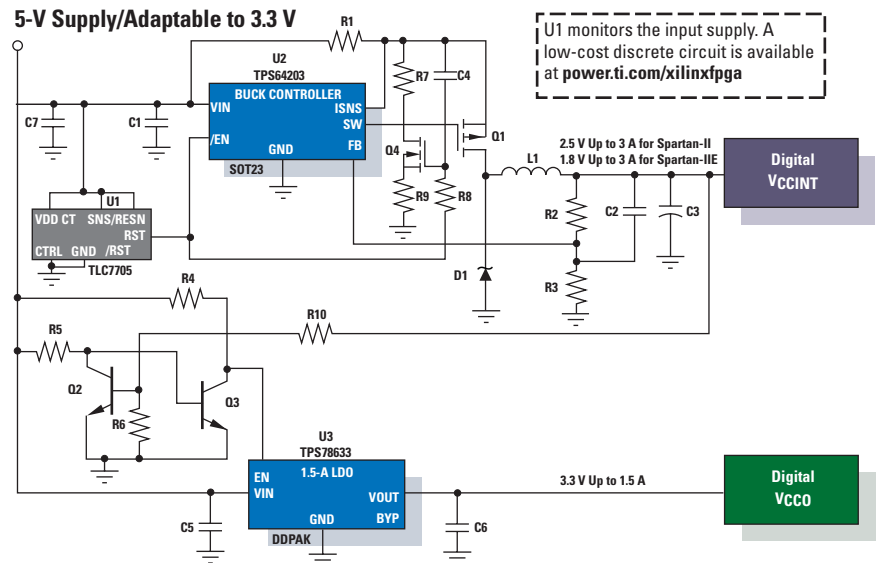


## Spartan™-IIE Design 3\*

### Switching DC/DC Controller-Based, 3-A $V_{CCINT}$ Solution

- Tiny SOT-23 switching DC/DC controller (U2) delivers up to 3 A at ultra-low cost.
- U1 monitors the input supply.
- $V_{CCINT}$  soft-starts from internal soft-start of U2.
- Sequence is  $V_{CCINT}$  then  $V_{CCO}$ .
- Size Q1 for the appropriate amount of current up to 3 A.
- Current sense resistor R1 gives more precise current limit; omit and connect ISNS to drain of Q1 to save cost and space.
- Reduce cost by using lower current LDOs from the TPS79xxx family for U3.
- Adapt to 3.3-V supply:
  - Omit U3 circuit
  - Replace TLC7705 with TLC7733

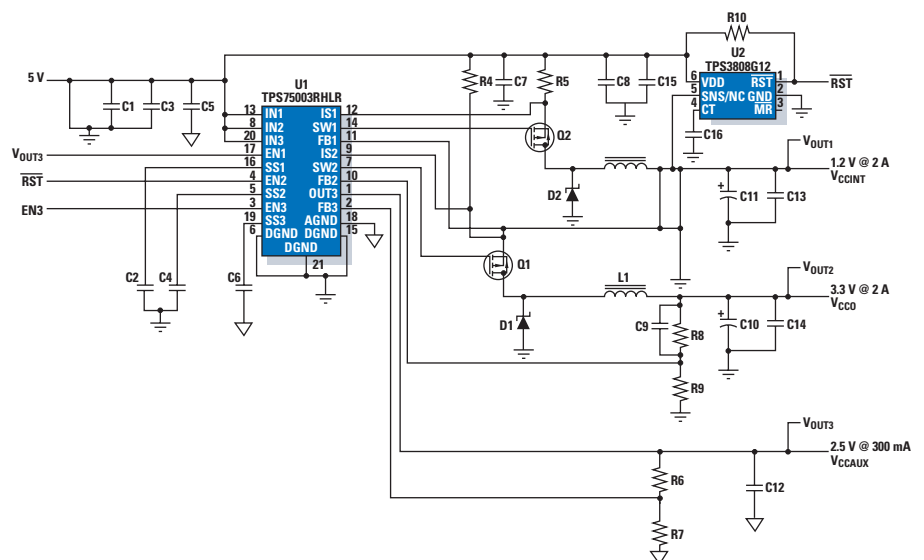
\*For Spartan-II, see [power.ti.com/xilinxfpga](http://power.ti.com/xilinxfpga)



## Spartan™-3/3E/3L Design 1

### Triple Supply with External Sequencing Provides 2 A for $V_{CCINT}$

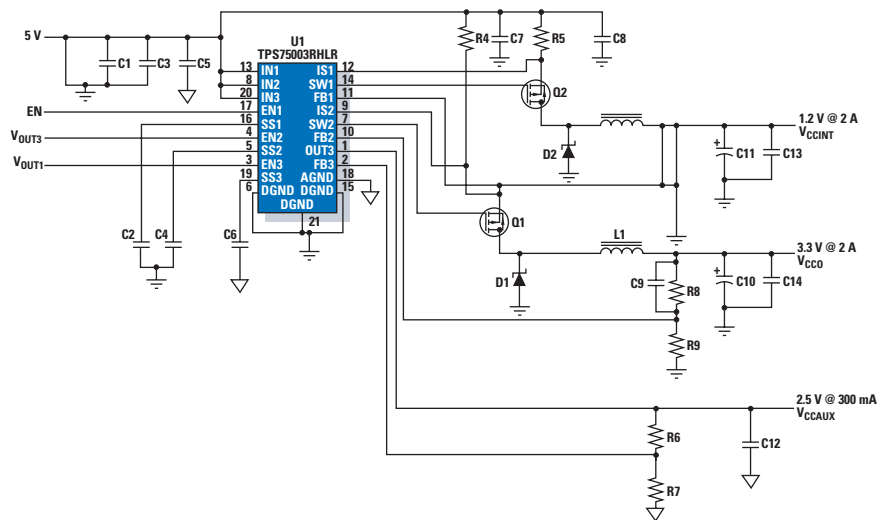
- TPS75003 has two, up to 95% efficient, up to 3-A buck controllers and one 300-mA LDO in a condensed 20-pin QFN package.
- External capacitor controlled soft-start for all 3 supplies.
- Soft-start sequence is  $V_{CCAUX}$ ,  $V_{CCINT}$ , then  $V_{CCO}$  with help from the TPS3808 supervisor.
- TPS3803 supervisor is needed because the 1.2-V  $V_{CCINT}$  cannot drive the DC/DC of EN2, which needs 1.4 V.
- Easily redesigned for  $V_{IN} = 3.3$  V and/or other output power levels with design software.



## Spartan™-3/3E/3L Design 2

### Triple Supply Provides 2 A for $V_{CCINT}$

- TPS75003 has two, up to 95% efficient, up to 3-A buck controllers and one 300-mA LDO in a condensed 20-pin QFN package.
- External capacitor controlled soft-start for all 3 supplies.
- Start-up sequence is  $V_{CCINT}$ ,  $V_{CCAUX}$ , then  $V_{CCO}$ , but can be changed by altering the EN pin connections.
- Easily redesigned for  $V_{IN} = 3.3\text{ V}$  and/or other output power levels with design software.
- See [power.ti.com/xilinxfpga](http://power.ti.com/xilinxfpga) for more designs.

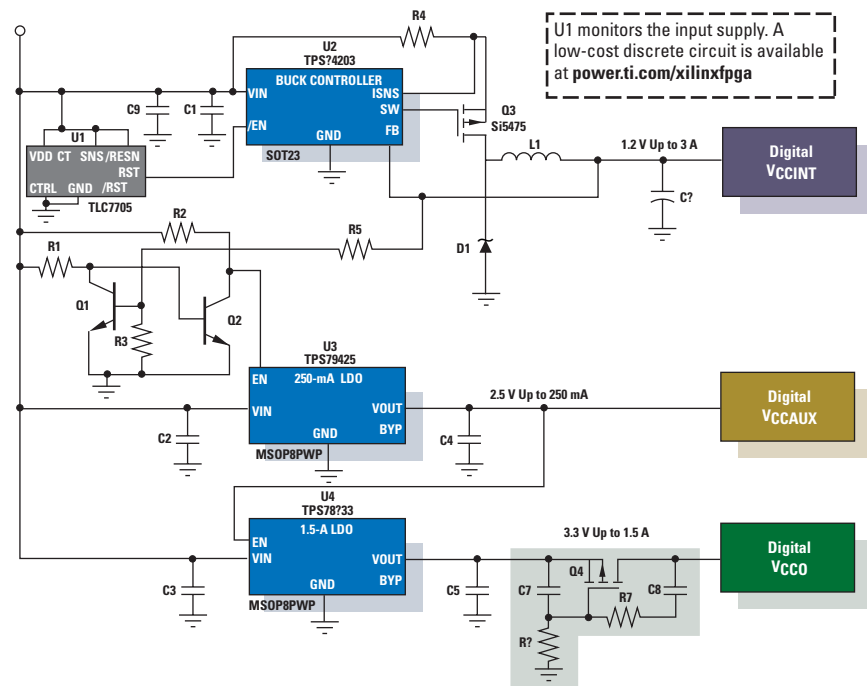


## Spartan™-3/3E/3L Design 3

### Switching DC/DC Controller-Based, 3-A $V_{CCINT}$ Solution

- Tiny SOT-23 switching DC/DC controller (U2) delivers up to 3 A at ultra-low cost.
- U1 monitors the input supply.
- $V_{CCINT}$  soft-starts from internal soft-start of U2.  $V_{CCO}$  soft-starts using Q4 circuitry with U4.
- Sequence is  $V_{CCINT}$  then  $V_{CCAUX}$  then  $V_{CCO}$ , but can be changed by altering the EN pin connections.
- Size Q3 for the appropriate amount of current up to 3 A.
- Current sense resistor R4 gives more precise current limit; omit and connect ISNS to drain of Q3 to save cost and space.
- Reduce cost by using lower current LDOs from the TPS79xxx family for U3, U4.
- Adapt for 3.3-V input supply:
  - Omit U4 circuit
  - Replace TLC7705 with TLC7733

5-V Input Supply/Adaptable to 3.3 V



### 3.3 V Configuration

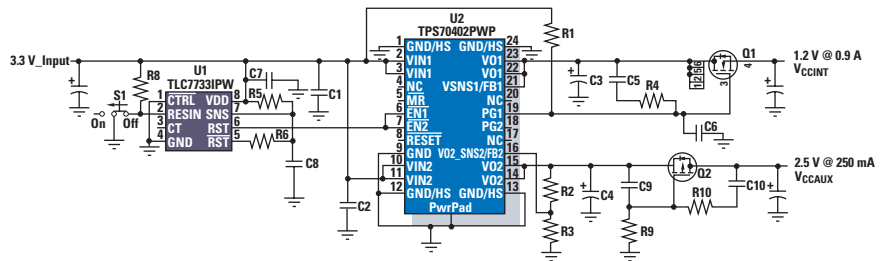
The Spartan-3 configuration and JTAG ports commonly use signals with a 2.5-V swing. Alternatively, it is possible to use 3.3-V signals simply by adding a few external resistors. The 3.3-V signals can cause a reverse current that flows from certain configuration and JTAG input pins, through the FPGA, to the  $V_{CCAUX}$  power rail. It is necessary to limit this current to 10 mA (or less) per pin, and to manage the reverse current flowing out of the  $V_{CCAUX}$  pins. Please see the web for solution recommendations.



## Spartan™-3/3E/3L/ Design 4 Dual LDO-Based, 900-mA $V_{CCINT}$ Solution

- Dual channel LDO in PowerPAD™ package saves cost and space.
- U1 monitors the input rail supply.
- Q1 and Q2 provide monotonic soft-start to  $V_{CCINT}$  and  $V_{CCAUX}$ .
- Soft-start provides sequencing  $V_{CCINT}$  then  $V_{CCAUX}$ .
- U2 is limited to 2 W @  $T_A = 55^\circ\text{C}$  and no airflow, due to power dissipation.

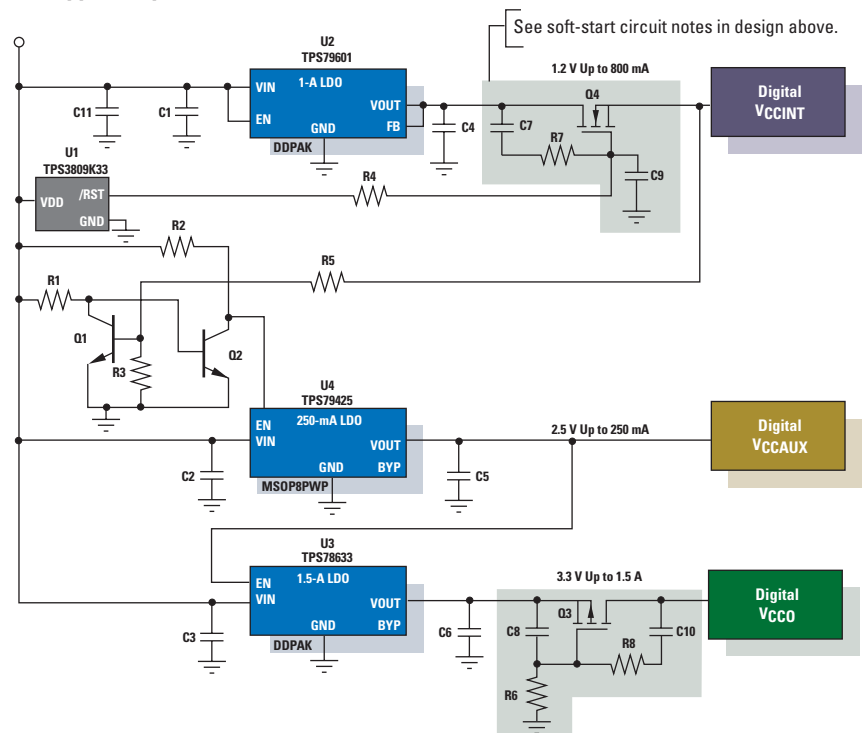
### 3.3-V Input Supply



## Spartan™-3/3E/3L Design 5 Single-Channel LDO-Based, 800-mA to 1.4-A $V_{CCINT}$ Solution

- Independent linear regulators allow higher power dissipation than an integrated dual-channel solution.
- Linear regulator solution saves cost and space over a switching DC/DC solution.
- U1 monitors the input supply.
- Q3 and Q4 provide monotonic soft-start to  $V_{CCINT}$  and  $V_{CCO}$ .
- Sequence is  $V_{CCINT}$  then  $V_{CCAUX}$  then  $V_{CCO}$ , but can be changed by altering the EN pin connections.
- Reduce cost by using lower current LDOs from the TPS79xxx family for U2, U3, U4.
- Adapt for 3.3-V input supply:
  - Omit U3 circuit
  - U2 is shown current limited to 800 mA @  $T_A = 55^\circ\text{C}$  given a 5-V input supply and no airflow, due to power dissipation. With a 3.3-V supply, U2 will support up to 1.4 A if changed to a TPS78601 1.5-A LDO.
  - Replace TPS3809K33 with TPS3809L30
  - Resize R4

### 5-V Supply/Adaptable to 3.3 V

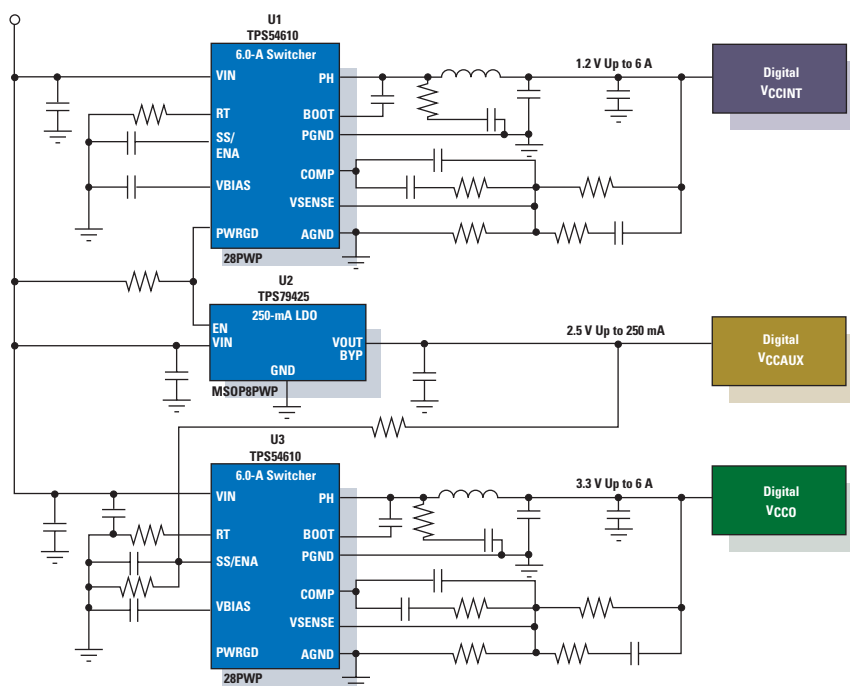


For 3.3-V configuration, see page 5.

## Spartan™-3/3E/3L Design 6 Switching DC/DC Converter-Based, 6-A $V_{CCINT}$ Solution

- Highly efficient  $V_{CCINT}$  and  $V_{CCO}$  rails up to 6 A. Interchange any of the TPS54x10 family of parts for different current levels from 1.5 A to 9 A. (See page 16 for pin compatibility).
- SWIFT™ (Switcher with Integrated FET) TPS54610 adjustable design allows use of smaller inductor, ceramic capacitors.
- Fixed TPS5461x 1.2-V and 3.3-V design with internal compensation and tantalum capacitors available.
- Use SWIFT design software to customize external components, or see the web for complete schematics.
- Integrated UVLO monitors input supply and integrated soft-start of U1/U3.
- Sequence is  $V_{CCINT}$  then  $V_{CCAUX}$  then  $V_{CCO}$ , but can be changed by altering the EN pin connections.
- Additional  $V_{CCO}$  rails easily added and sequenced using TPS54xxx PWRGD feature and enable.
- Adapt for 3.3-V supply:
  - Omit U3 circuit

### 5-V Input Supply/Adaptable to 3.3 V

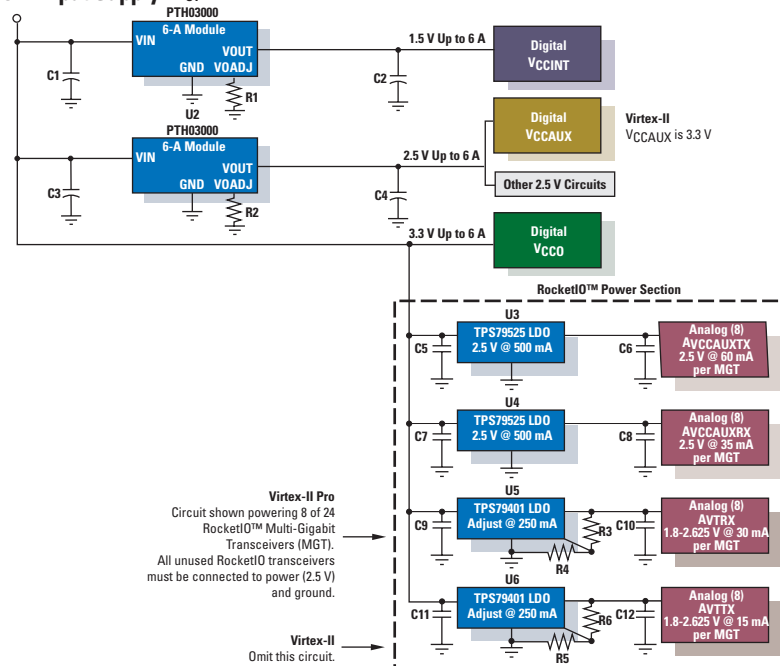


For 3.3-V configuration, see page 5.

## Virtex™-II/ Virtex-II Pro™ Design 1 Module-Based, 6-A $V_{CCINT}$ Solution

- Simple to use plug-in modules.
- Highly efficient  $V_{CCINT}$  and  $V_{CCO}$  rails.
- Additional  $V_{CCO}$  rails easily added.
- Interchange modules to support:
  - 6 A to 30 A
  - 5.0-V or 12-V input supply
  - Minimum input and output capacitors may change depending on application
- Reduce cost by using lower current LDOs from the TPS79xxx family for the RocketIO™ power section.

### 3.3-V Input Supply



#### RocketIO™ Power Section

$AV_{CCAUXTX}$ ,  $V_{CCAUXRX}$ ,  $AV_{TRX}$ , and  $AV_{TTX}$  are shown powered by independent linear regulators but they may all be powered by the same linear regulator, if desired. See TPS79xxx and TPS786xx LDO selection guide (see page 16).

**Virtex-II Pro**  
Circuit shown powering 8 of 24 RocketIO™ Multi-Gigabit Transceivers (MGT). All unused RocketIO transceivers must be connected to power (2.5 V) and ground.

**Virtex-II**  
Omit this circuit.

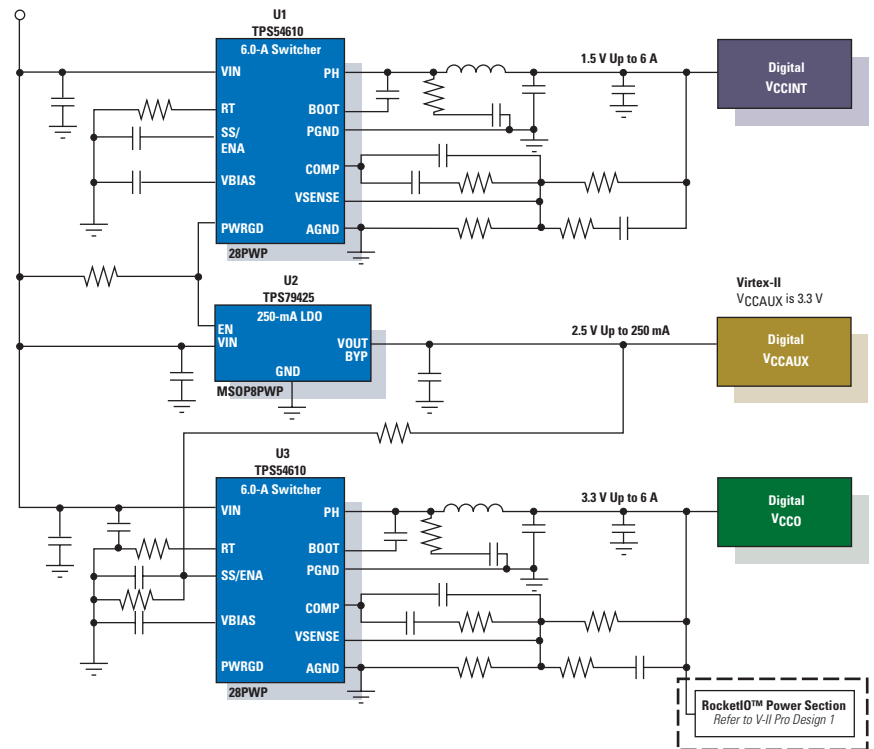


## Virtex™-II/ Virtex-II Pro™ Design 2

### Switching DC/DC Converter-Based 6-A $V_{CCINT}$ Solution

- Highly efficient  $V_{CCINT}$  and  $V_{CCO}$  rails up to 6 A. Interchange any of the TPS54x10 family of parts for different current levels from 1.5 A to 9 A. (See page 16 for pin compatibility.)
- SWIFT™ (Switcher with Integrated FET) TPS54610 adjustable design allows use of smaller inductor, ceramic caps.
- Fixed TPS5461x 1.5-V and 3.3-V design with internal compensation and tantalum caps available.
- Use SWIFT design software to customize external components, or see the web for complete schematics.
- Integrated UVLO monitors input supply and external capacitor controlled U1/U3.
- Sequence is  $V_{CCINT}$ ,  $V_{CCAUX}$  then  $V_{CCO}$ , but can be changed by altering the SS pin connections.
- Additional  $V_{CCO}$  rails easily added and sequenced using TPS54xxx PWRGD feature and ENABLE.
- Adapt for 3.3-V supply:
  - Omit U3 circuit

5-V Supply/Adaptable to 3.3 V

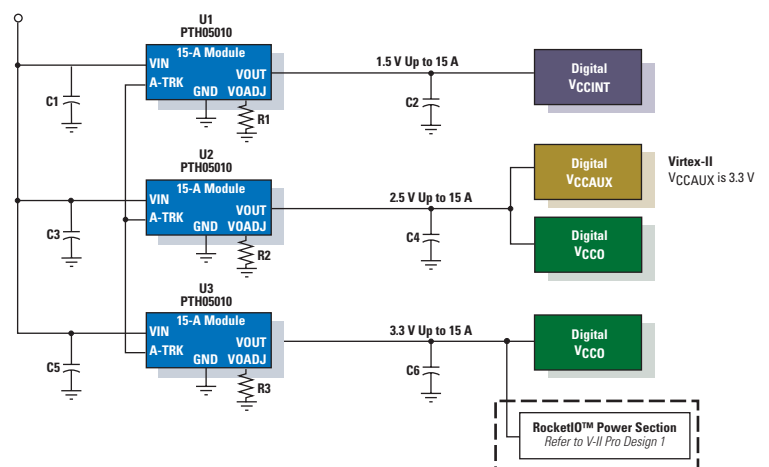


## Virtex™-II/ Virtex-II Pro™ Design 3

### Modular-Based 15-A $V_{CCINT}$ Solution

- Simple to use plug-in modules.
- Powers one or multiple FPGAs.
- Highly efficient  $V_{CCINT}$  and  $V_{CCO}$  rails.
- Integrated UVLO monitor input supply and fixed soft-start of U1/U2/U3 provides monotonic rise.
- Auto-Track™ connected as shown provides simultaneous sequencing. Supply voltage supervisors can be added for sequential sequence. See the web for alternate implementations.
- Interchange modules to support:
  - 6 A to 30 A
  - 3.3-V or 12-V input supply
  - Minimum input and output capacitors may change depending on application

5-V Supply/Adaptable to 3.3 V or 12 V

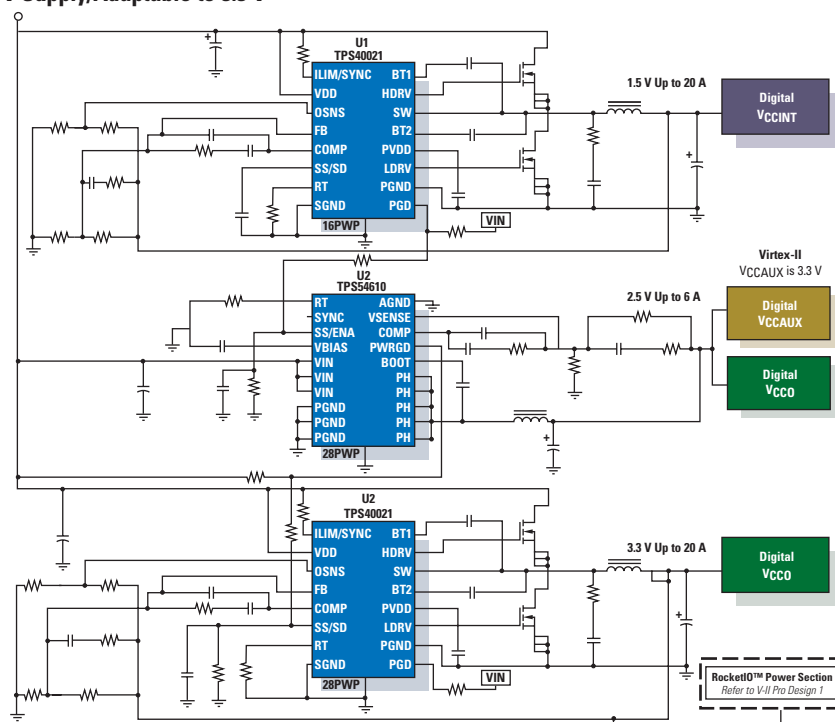


## Virtex™-II/ Virtex-II Pro™ Design 4

### Low-Voltage Switching DC/DC Controller-Based, 20-A $V_{CCINT}$ Solution

- Powers one or multiple FPGAs.
- Highly efficient  $V_{CCINT}$  and  $V_{CCO}$  rails up to 20 A.
- Flexible controller design allows optimization for size, power dissipation and cost.
- Use TPS40K™ and SWIFT™ design software to customize designs, or see the web for complete schematics.
- Adjustable TPS541x allows use of smaller inductor, ceramic capacitors.
- Fixed TPS5461x design with internal compensation and tantalum caps available.
- Interchange any of the TPS54x10 SWIFT family of parts for different current levels from 1.5 A to 9 A. (See page 16 for pin-pin compatibility.)
- External capacitor controlled soft-start of U1, U2 and U3 provides monotonic rise.
- Sequence is  $V_{CCINT}$ ,  $V_{CCAUX}$  then  $V_{CCO}$ , but can be changed by altering the SS connections.
- Additional  $V_{CCO}$  rails easily added and sequenced.
- Adapt for 3.3 V supply:
  - Omit U3 circuit

5-V Supply/Adaptable to 3.3 V

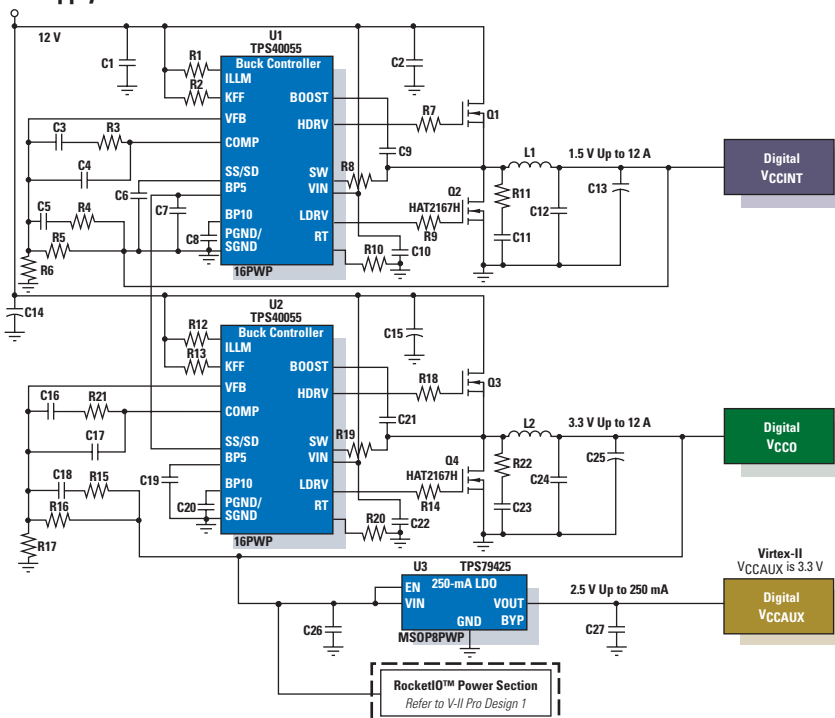


## Virtex™-II/ Virtex-II Pro™ Design 5

### High-Voltage Switching DC/DC Controller-Based, 12-A $V_{CCINT}$ Solution

- Powers one or multiple FPGAs.
- Highly efficient  $V_{CCINT}$  and  $V_{CCO}$  rails up to 12 A.
- Flexible controller design allows optimization for size, power dissipation, and cost.
- Use TPS40K™ design software to customize designs, or see the web for complete schematics.
- External capacitor controlled soft-start provides monotonic rise and integrated UVLO of U1/U2 monitors input supply.
- Sequence is  $V_{CCINT}$ ,  $V_{CCO}$  then  $V_{CCAUX}$ .
- Additional  $V_{CCO}$  rails easily added and sequenced.
- Reduce cost by using lower current LDOs from the TPS79xxx family for U3.

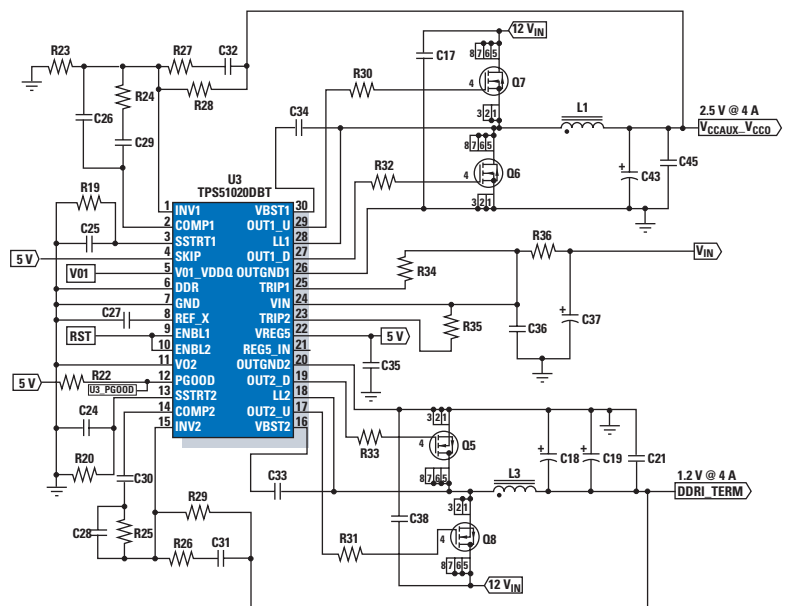
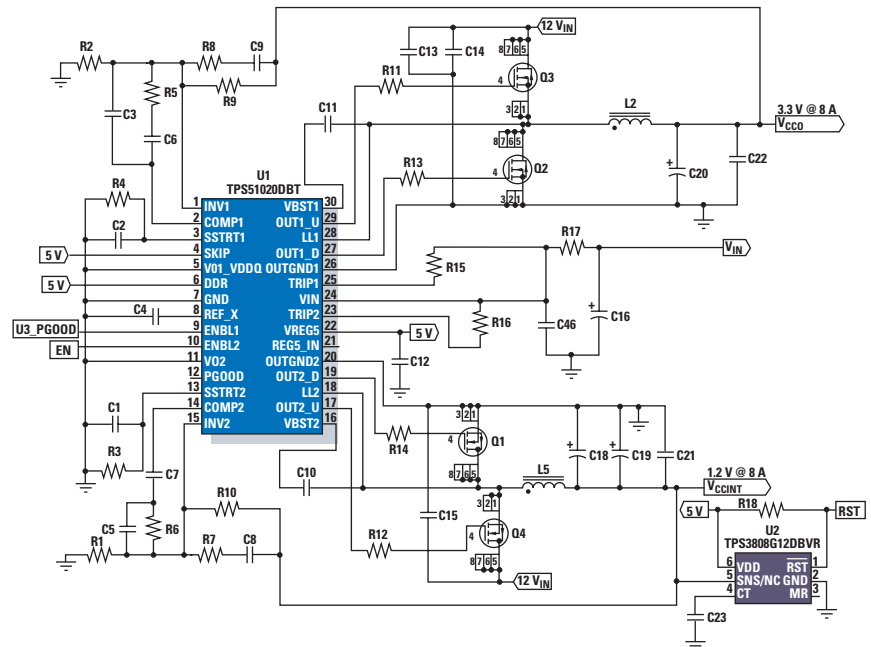
12-V Supply



## Virtex™-4 Design 1 and 2

Switching Dual DC/DC Controller, 8-A  $V_{CCINT}$  from  $V_{IN} = 12\text{-V}$  and 6-A  $V_{CCINT}$  from  $V_{IN} = 5$ 

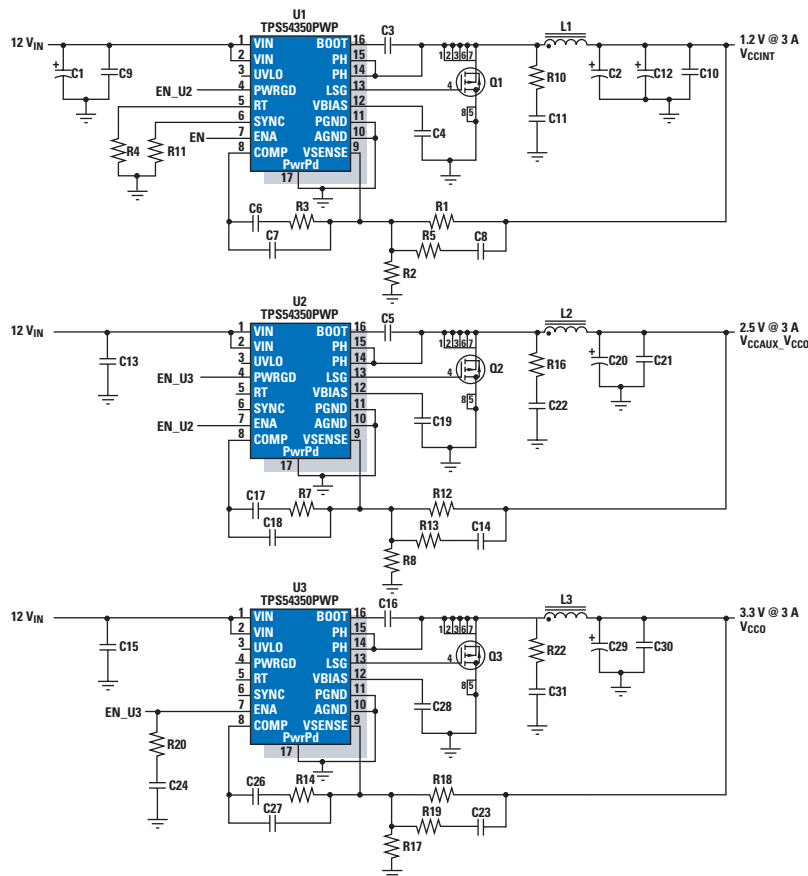
- Powers one or multiple FPGAs.
- Flexible dual controller (TPS51020) design allows optimization for input voltage (4.5 v to 28 V), output power, 2 size, power dissipation and/or cost.
- DDR termination provided.
- External capacitor controlled soft-start provides monotonic rise.
- Sequence is  $V_{CCINT}$ ,  $V_{CCAUX}$  and  $V_{CCO}$ .
- For a 5  $V_{IN}$  @ 6-A solution using TPS51020, please refer to (PR448) at: [www.ti.com](http://www.ti.com).
- Use TPS40K™ software for other output power requirements.



## Virtex™-4 Design 3

### SWIFT™ (TPS54350 Series) DC/DC Converter, 3-A $V_{CCINT}$ from $V_{IN} = 12\text{ V}$

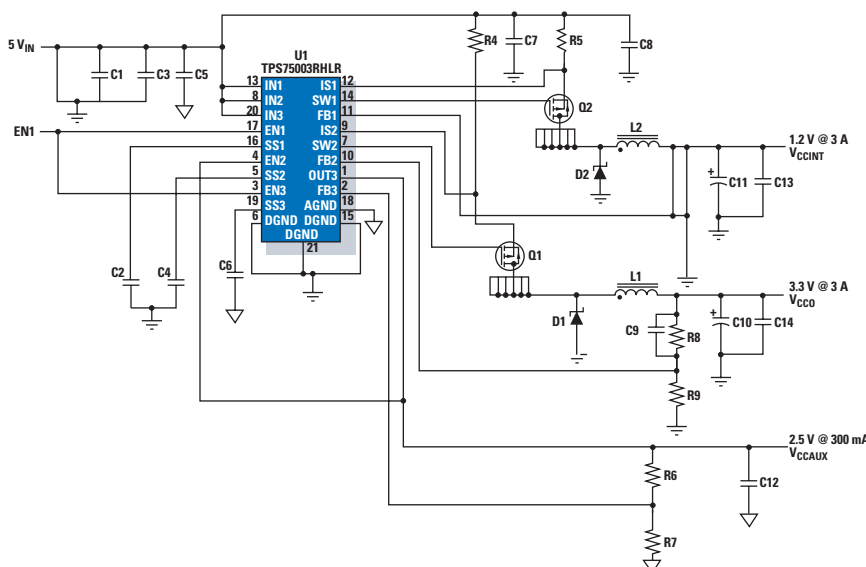
- Highly efficient  $V_{CCINT}$ ,  $V_{CCAUX}$  and  $V_{CCO}$  up to 3 A.
- SWIFT™ (Switcher with Integrated FET) TPS54350 with fixed  $12\text{ V}_{IN}$ .
- External capacitor controlled soft-start provides monotonic rise.
- Sequence is  $V_{CCINT}$ ,  $V_{CCAUX}$  and  $V_{CCO}$ , but can be changed by altering EN pin connections.
- Additional  $V_{CCO}$  rails can be added and sequenced using TPS54350 PWRGD feature and ENABLE.
- Use SWIFT design software to customize external components.



## Virtex™-4 Design 4

### TPS75003 Triple Supply Provides 3-A $V_{CCINT}$ from $V_{IN} = 5\text{ V}$

- TPS75003 has two, up to 95%-efficient, up to 3-A buck controllers and one 300-mA LDO in a condensed 20-pin QFN package.
- External capacitor controlled soft-start for all three supplies.
- Start-up sequence is  $V_{CCINT}$ ,  $V_{CCAUX}$ , then  $V_{CCO}$ , but can be changed by altering the EN pin connections.
- Easily redesigned for  $V_{IN} = 3.3\text{ V}$  and/or other output power levels with design software.
- See [power.ti.com/xilinxfpga](http://power.ti.com/xilinxfpga) for more designs.

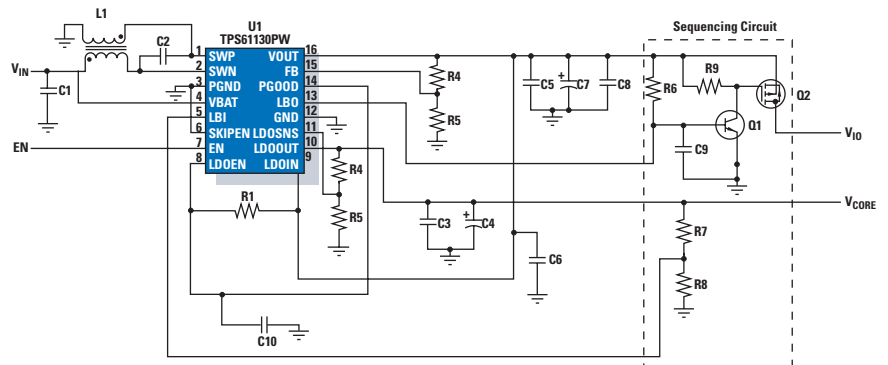


## CoolRunner™-II Design 1

### Single Li-Ion/Li-Pol Battery Power Source ( $V_{IN}$ 2.7 V - 4.2 V)

- Synchronous, up to 90%-efficient SEPIC converter with 300-mA output current from 1.8-V input.
- Integrated 200-mA reverse voltage protected LDO for core output voltage.
- Dual input or dual output mode (*optional*).
- Available in a 16-pin, QFN 4 mm x 4 mm or in a TSSOP-16 package.
- Adjust  $V_{IO}$  levels by sizing R4 and R5 appropriately (*See table below*).

Voltage (V)	R4	R5 (k)
1.5	909 k	453
1.8	909 k	348
2.5	1.0 M	249
3.3	1.0 M	178

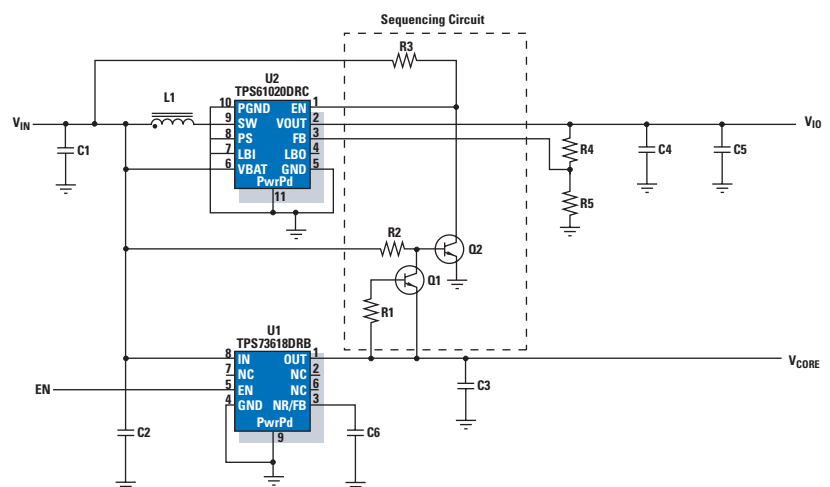


## CoolRunner™-II Design 2

### Dual NiMH/NiCD/Alkaline Battery Power Source ( $V_{IN}$ 1.8 V - 3.0 V)

- 96%-efficient synchronous boost converter providing 500 mA with a 1.8-V input.
- Cap-free LDO providing 400 mA.
- Sequencing of  $V_{CORE}$  then  $V_{IO}$  for reliable startup.
- Adjustable  $V_{IO}$  with R4 and R5. (*See table below*).

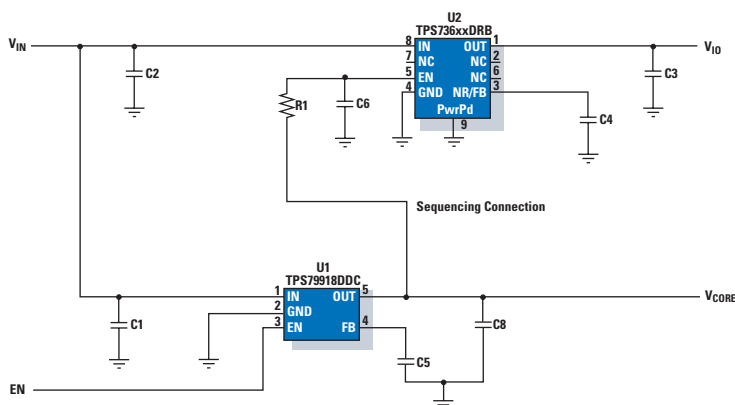
Voltage (V)	R4 (k)	R5 (M)
2.5	249	1.0
3.3	178	1.0



## CoolRunner™-II Design 3

### Single Li-Ion, Li-Poly or 2/3 Cell in Series NiHm, Ni-CD, Alkline ( $V_{IN}$ 2.7 V - 5.5 V)

- TPS736xx LDO provides 400-mA current for  $V_{IO}$  in a small 8-pin SON.
- TPS79918 LDO provides 200-mA for  $V_{CORE}$ .
- Sequence with EN pin on TPS736xx.
- Adjustable  $V_{IO}$  with 1.5-V, 1.8-V, 2.5-V versions of the TPS736xx.

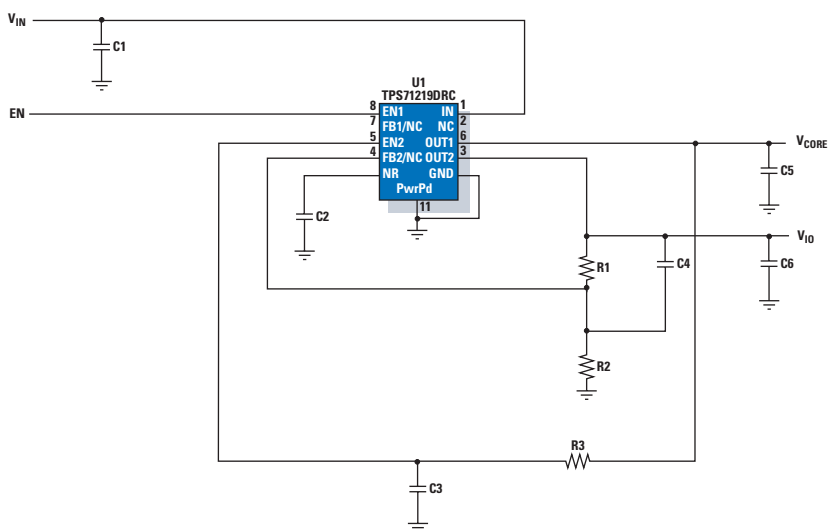


## CoolRunner™-II Design 4

### Single Li-Ion /Li-Poly Battery Power Source ( $V_{IN}$ 2.7 V - 4.2 V)

- Dual 250 mA @ 3-V LDO solution in a small 10-pin package.
- Simple sequencing of  $V_{CORE}$  then  $V_{IO}$  with EN pin.
- Adjustable  $V_{IO}$  with R1, R2, and C4  
(See table below).

Voltage (V)	R4 (k)	R5 (k)	C4 (pF)
1.5	7.15	30.1	100
1.8	14	30.1	33
2.5	31.6	30.1	22





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[www.ti.com/analoglit](http://www.ti.com/analoglit)

TI has a full line of Power Management literature to help in your design process:

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- *Plug-In Power Product Selector Guide*
- *Portable Power Management Sine On*
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- |                     |          |
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| • MicroStar Junior™ | • SOT23  |
| • MSOP              | • SSOP   |
| • NanoFree™         | • TO-220 |
| • PBGA              | • TQFP   |
| • PDIP              | • TSOT   |
| • PLCC              | • TSSOP  |
| • PowerPAD™         | • TVSOP  |
| • QFN               |          |
| • QFP               |          |
| • QSOP              |          |
| • SC70              |          |
| • SIP               |          |
| • SOIC              |          |



**Pb-Free**

## Selection Guides

### Low Dropout Regulators (LDO)

Device <sup>1</sup>	I <sub>O</sub> (mA)	V <sub>DO</sub> @ I <sub>O</sub> (mV)	I <sub>q</sub> (μA)	Output Options		Min V <sub>IN</sub>	Max V <sub>IN</sub>	Accuracy (%)	Packages				Features <sup>2</sup>	C <sub>0</sub> <sup>3</sup>	Comments	Price <sup>4</sup>
				Fixed Voltage (V) (V)	Adj.				SOT23	MSOP	SOT223	DDPAK				
Positive Voltage, Single Output Devices																
TPS793xx	200	77	170	1.8, 2.5, 2.8, 2.85, 3.0, 3.3, 4.75	1.2 to 5.5	2.7	5.5	2	✓				EN, BP	2.2 μF C	RF Low Noise, High PSRR	0.28
TPS794xx	250	145	170	1.8, 2.5, 2.8, 3.0, 3.3	1.2 to 5.5	2.7	5.5	3		✓		✓	EN, BP	2.2 μF C	RF Low Noise, High PSRR	0.65
TPS795xx	500	105	265	1.6, 1.8, 2.5, 3.0, 3.3	1.2 to 5.5	2.7	5.5	2				✓	EN, BP	1 μF C	RF Low Noise, High PSRR	1.05
TPS796xx	1000	200	265	1.8, 2.5, 2.8, 3.0, 3.3	1.2 to 5.5	2.7	5.5	2				✓	EN, BP	1 μF C	RF Low Noise, High PSRR	1.10
TPS786xx	1500	390	265	1.8, 2.5, 2.8, 3.0, 3.3	1.2 to 5.5	2.7	5.5	2				✓	EN, BP	1 μF C	RF Low Noise, High PSRR	1.35
UC382-x	3000	350	6 mA	1.5, 2.1, 2.5	1.20 to 6.0	1.7	7.5	1				✓	—	100 μF T	Separate V <sub>BIAS</sub>	2.70

<sup>1</sup>xx represents the voltage option. For example, 33 represents the 3.3-V option. The adjustable output voltage option is represented by 01.

<sup>2</sup>EN = Active High Enable, BP = Bypass Pin for noise reduction capacitor.

<sup>3</sup>T = Tantalum, C = Ceramic output capacitor. TPS795/796/786xx minimum C<sub>O</sub> is only 1 μF but 2.2 μF was used in the reference designs to minimize the bill of materials since the input capacitor requirement is 2.2 μF.

<sup>4</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

### Dual Output LDOs

Device	I <sub>O1</sub> (mA)	I <sub>O2</sub> (mA)	V <sub>DO1</sub> @ I <sub>O1</sub> (mV)	V <sub>DO2</sub> @ I <sub>O2</sub> (mV)	I <sub>q</sub> (μA)	Output Options		Accuracy (%)	PWP Package	Min V <sub>O</sub>	Max V <sub>O</sub>	Features								Description	Price <sup>2</sup>
						Fixed Voltage (V)	Adj.					/EN	PG	SVS	Seq	Low Noise	Min V <sub>IN</sub>	Max V <sub>IN</sub>	C <sub>O</sub> <sup>1</sup>		
TPS703xx	2000	1000	160	—	185	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5.5	✓	✓	✓	✓	✓	2.7	5.5	22 μF T	Dual Output LDO with Sequencing	2.35
TPS704xx	2000	1000	160	—	185	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5.5	✓	✓	✓	✓		2.7	5.5	22 μF T	Dual Output LDO with Independent Enable	2.35

<sup>1</sup>T = Tantalum output capacitor.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

### Switching DC/DC Converters

Device	I <sub>OUT</sub> (mA)	V <sub>IN</sub> (V)	Adj (V)	V <sub>OUT</sub> Fix (V)	V <sub>OUT</sub> Efficiency %	Switching Frequency (max) (kHz)	Quiescent Current (typ) (mA)	Features					Package TSSOP	EVM	Price <sup>1</sup>
								Shutdown	Power Good	Dual Input Bus (3.3, 2.5 V)	Current Limit	Thermal Limit			
SWIFT™ Step Down (Buck) Converters — up to 9 A															
TPS54110	1500	3.0 to 6.0	0.9 to 4.5	—	90	700	3.6	✓	✓		✓	✓	20	✓	2.00
TPS54310	3000	3.0 to 6.0	0.9 to 4.5	—	90	700	6.2	✓	✓		✓	✓	20	✓	2.35
TPS54311	3000	3.0 to 6.0	—	0.9	90	700	6.2	✓	✓		✓	✓	20		2.35
TPS54312	3000	3.0 to 6.0	—	1.2	90	700	6.2	✓	✓		✓	✓	20		2.35
TPS54313	3000	3.0 to 6.0	—	1.5	90	700	6.2	✓	✓		✓	✓	20		2.35
TPS54314	3000	3.0 to 6.0	—	1.8	90	700	6.2	✓	✓		✓	✓	20	✓	2.35
TPS54315	3000	3.0 to 6.0	—	2.5	90	700	6.2	✓	✓		✓	✓	20		2.35
TPS54316	3000	3.0 to 6.0	—	3.3	90	700	6.2	✓	✓		✓	✓	20		2.35
TPS54350	3000	4.5 to 20	0.9 to 12	—	85	700	9	✓	✓		✓	✓	16	✓	2.05
TPS54610	6000	3.0 to 6.0	0.9 to 4.5	—	90	700	11	✓	✓		✓	✓	28	✓	3.35
TPS54611	6000	3.0 to 6.0	—	0.9	90	700	11	✓	✓		✓	✓	28		3.35
TPS54612	6000	3.0 to 6.0	—	1.2	90	700	11	✓	✓		✓	✓	28		3.35
TPS54613	6000	3.0 to 6.0	—	1.5	90	700	11	✓	✓		✓	✓	28		3.35
TPS54614	6000	3.0 to 6.0	—	1.8	90	700	11	✓	✓		✓	✓	28	✓	3.35
TPS54615	6000	3.0 to 6.0	—	2.5	90	700	11	✓	✓		✓	✓	28		3.35
TPS54616	6000	3.0 to 6.0	—	3.3	90	700	11	✓	✓		✓	✓	28		3.35
TPS54810	8000	4.0 to 6.0	0.9 to 4.5	—	85	700	11	✓	✓		✓	✓	28	✓	3.95
TPS54910	9000	3.0 to 4.0	0.9 to 2.5	—	90	700	11	✓	✓		✓	✓	28	✓	4.20
TPS54974	9000	2.2 to 4.0	0.2 to 2.5	—	90	700	11	✓	✓	✓	✓	✓	28	✓	4.20

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

New products appear in **BOLD RED**.

## Selection Guides

### Switching DC/DC Controllers

Device	V <sub>IN</sub> (V)	V <sub>O</sub> (max) (V)	V <sub>O</sub> (min) (V)	V <sub>ref</sub> Tol (%)	Driver Current (A)	Output Current Range (A)	Multiple Outputs	Adaptive Voltage Positioning	Protection <sup>1</sup>	Comments	Price <sup>2</sup>
<b>Performance Processor Power Supply Controllers (Synchronous Rectification)</b>											
TPS64200	1.8 to 6.5	6.5	1.2	2	0.150	0 to 3	No	No	OCP, UVLO	Non-sync buck in SOT-23	0.55
TPS40021	2.25 to 5.5	4	0.7	1	1	10 to 20	No	No	OCP, UVLO	Enhanced flexibility with user programmability	1.15
TPS40055	8 to 40	30	0.7	1	1	3 to 15	No	No	OCP, UVLO	Wide input range sync buck, source/sink	1.35
TPS40061	10 to 55	40	0.7	1	1	1 to 8	No	No	OCP, UVLO	Wide input range sync buck, source/sink	1.40

<sup>1</sup>OCP = over-current protection; UVLO = under-voltage lockout.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

### Plug-In Power Solutions

Device <sup>1</sup>	Input Bus Voltage (V)	P <sub>OUT</sub> or I <sub>OUT</sub> (A)	Isolated Outputs	V <sub>O</sub> Range (V)	V <sub>O</sub> Adjustable	Price <sup>2</sup>
<b>Non-Isolated Single Positive Output</b>						
PTH03010/20/30/50/60	3.3	15, 22, 30, 6, 10	No	0.8 to 2.5	Yes	11.60, 18.15, 25.00, 6.90, 9.80
PTH05010/20/30/50/60	5	15, 22, 30, 6, 10	No	0.8 to 3.6	Yes	11.60, 18.15, 25.00, 6.90, 9.80
PTH12010/20/30/50/60	12	12, 18, 26, 6, 8	No	1.2 to 5.5	Yes	11.60, 18.15, 25.00, 6.90, 9.80

<sup>1</sup>See [power.ti.com](http://power.ti.com) for a complete product offering.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

### Supply Voltage Supervisors (SVS)

Device	Number of Supervisors	Supervised Voltages	Packages	I <sub>DD</sub> (typ) (μA)	Time Delay (ms)	Watchdog Timer WDT (sec)	Manual Reset Input/MR	Active-High Reset Output	Reset Output Topology <sup>1</sup>	Comments	Price <sup>2</sup>
TPS3809	1	2.5/3.0/3.3/5.0	SOT-23	9	200	—	—	—	PP <sup>1</sup>	Small, low cost	0.29
TLC77xx	1	Adj./2.5/3.3/3.0/5.0	SO-8, DIP-8, TSSOP-8	9	Prog	—	—	✓	PP	Universal SVS with broad voltage range and both active-low and active-high reset	0.65
TPS3808	1	Adj./1.0/1.2/1.5/1.8/2.5/3.0/3.3/5.0	SOT-23	24	Prog	—	✓	—	OD	—	0.70

<sup>1</sup>PP = push-pull; OD = open drain.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

### Active Bus Terminator<sup>1</sup> (DDR) Converter (with Integrated FETs) Solutions

Device	I <sub>OUT</sub> (mA)	V <sub>IN</sub> (V)	Adj. (V)	V <sub>OUT</sub> Efficiency %	Switching Frequency (max) (kHz)	Package TSSOP	EVM	Price <sup>2</sup>
TPS54372	3000	3.0 to 6.0	0.2 to 4.5	90	700	20	✓	2.35
TPS54672	8000	3.0 to 6.0	0.2 to 4.5	90	700	28	✓	3.35
TPS54872	8000	4.0 to 6.0	0.2 to 4.5	85	700	28	✓	3.95
TPS54972	9000	3.0 to 4.0	0.2 to 4.5	90	700	28	✓	4.20

<sup>1</sup>Tracks externally applied reference voltage.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

### Active Bus Terminator<sup>1</sup> (DDR) Controller (with External FETs) Solutions

Device	I <sub>OUT1</sub> (V <sub>DDQ</sub> ) (A)	I <sub>OUT2</sub> (V <sub>TT</sub> ) (A)	I <sub>OUT3</sub> (buf. V <sub>REF</sub> ) (mA)	V <sub>IN</sub> (V)	V <sub>OUT1</sub> (V <sub>DDQ</sub> ) Adj. (V)	V <sub>OUT2</sub> (V <sub>TT</sub> ) Fixed (V)	V <sub>OUT3</sub> (buf. V <sub>REF</sub> ) Fixed (V)	Switching Frequency Selectable (kHz)	Light Load Efficiency Mode	Selectable Output Discharge	Package TSSOP	Price <sup>2</sup>
TPS51020	10	5	3	4.5 V to 28 V	0.9 to 90% V <sub>IN</sub>	1/2 V <sub>DDQ</sub>	1/2 V <sub>DDQ</sub>	270, 360, 450	Yes	Yes	30	3.15

<sup>1</sup>Solution includes V<sub>DDQ</sub>, V<sub>TT</sub>, and buffered V<sub>REF</sub> outputs.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

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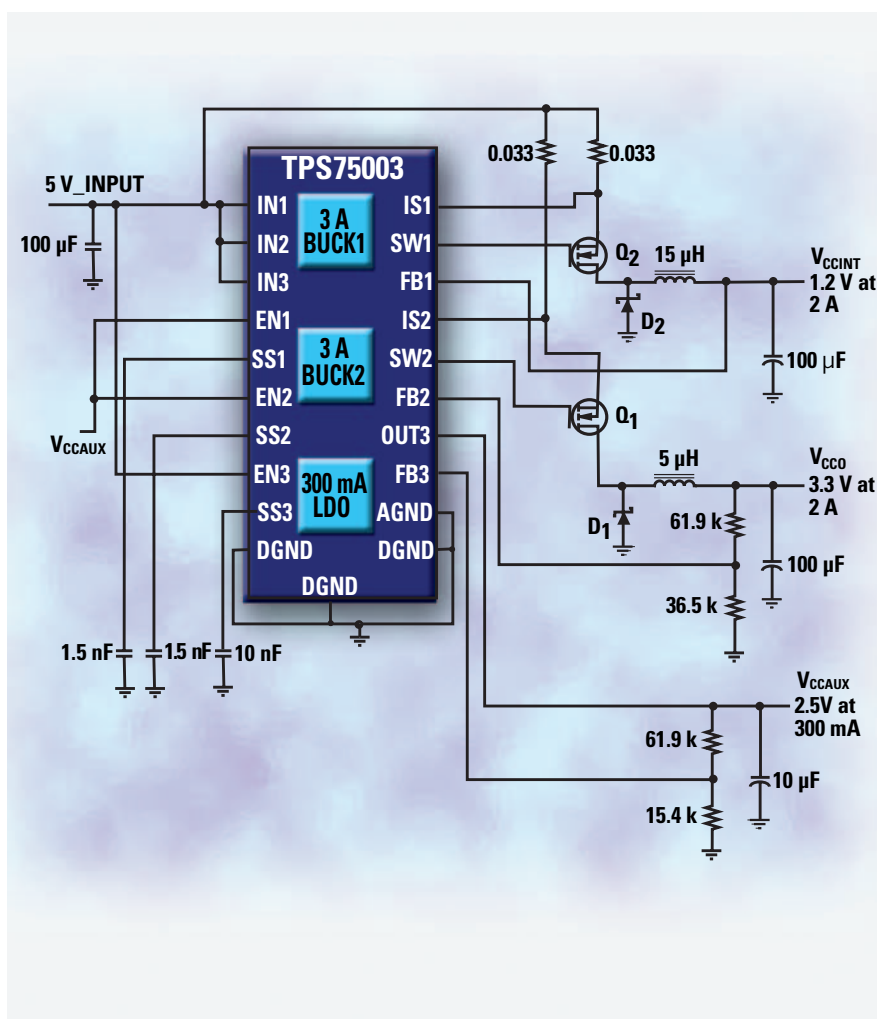
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## Triple Supply Powers Spartan™-3

The **TPS75003** power management IC for Xilinx's Spartan™-II/IIE/3 series of FPGAs integrates multiple functions to significantly reduce the number of external components required and simplify design. Applications include DSL modems, set-top boxes, plasma TV display panels and DVD players.

### Features

- Two 95%-efficient, 3-A buck controllers and one 300-mA LDO
- Adjustable output voltages from 1.2 V for bucks and from 1.0 V for LDO
- Input voltage range of 2.2 V to 6.5 V
- Independent soft-start for all three power supplies
- LDO stable with small ceramic output capacitor
- Independent enable for each supply for flexible sequencing
- 4.5 mm x 3.5 mm x 0.9 mm 20-pin, QFN package
- \$1.90: 1 K price

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